REMARKS

In the Official Action mailed on **19 October 2007**, the Examiner reviewed claims 1-45. Claims 1-45 were rejected on the ground of nonstatutory double patenting over claims 1-33 of USPN 6,928,508. Claims 1-45 were provisionally rejected on the ground of nonstatutory double patenting over copending Application No. 10/091,746. Claims 1-45 were rejected under 35 U.S.C. § 102(e) based on Craddock et al. (USPN 7,092,401 hereinafter "Craddock"). Claims 34-37 were rejected under 35 U.S.C. § 103(a) based on Craddock and in view of the well-known art.

Double Patenting Rejection

Claims 1-45 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-33 of U.S. Patent No. 6,928,508 and claims 1-42 of copending Application No. 10/091,746.

Applicant respectfully submits the attached terminal disclaimer with respect to U.S. Patent No. 6,928,508 to obviate the rejection under obviousness-type double patenting.

However, as described by Applicant in a phone conversation with Examiner on 19 December 2007, Application No. 10/091,746 has been abandoned. Hence, Applicant respectfully requests the withdrawal of the double patenting rejection based on Application No. 10/091,746.

Rejections under 35 U.S.C. § 102(e) and 35 U.S.C. §103(a)

Claims 1-45 were rejected as being anticipated by Craddock. Claims 34-37 were rejected as being unpatentable under Craddock in view of the well-known art. Applicant respectfully disagrees because Craddock does not

disclose sharing a single contiguous memory between multiple queue pairs and virtual lanes.

Examiner avers that Craddock discloses a shared memory in col. 12, line 36 and a single contiguous memory structure shared by multiple queue pairs and virtual lanes in col. 9, line 67 and Fig. 4 (see page 6, the last paragraph of the office action). However, Applicant points out that Craddock is not a single contiguous memory structure shared by multiple queue pairs and virtual lanes. Instead each queue pair has its own send work queue and receive work queue (see col. 11, ll. 24-26 of Craddock). The work queue element (WQE in Fig. 4 of Craddock) contains references to several data segments, and **each data segment** contains a **virtually** contiguous memory region (see col. 9, ll. 63-67 of Craddock). This virtually contiguous memory region is different from the **single contiguous memory structure shares by multiple queue pairs and virtual lanes** taught by instant application for at least the following reasons. First, the Craddock memory is virtually contiguous which means that the physical memory that contains the data segment could be fragmented. Second, the Craddock memory is only virtually contiguous for **each data segment**, while there is no contiguous relationship among different data segments as shown in Fig. 4 of Craddock. In addition, col. 12, ll. 36 of Craddock only discloses that the end-to-end states that keep track of sequence numbers, acknowledgments and time-out values are shared by all queue pairs. It does not disclose a memory structure shared by queue pairs.

Furthermore, Craddock discloses that each queue pair has its own sending and receiving work queues, each of which has its dedicated queue structure and memory page (see col. 16, ll. 60-67 of Craddock). The dedicated queue for each queue pair results in an inefficient use of memory space because memory is allocated for queue pairs regardless of whether the queue pairs are active or not (see page 2-3 ll. 23-5 of the instant application).

In contrast, the embodiments of the present invention are directed to sharing a single contiguous memory structure among multiple queue pairs and virtual lanes (see page 4, ll. 13-26 of the instant application), wherein a given packet payload is stored contiguously in the memory for the outbound communications (see page 16, ll. 7-9 of the instant application). There is nothing in Craddock, either explicit or implicit, that discloses sharing a single contiguous memory structure among multiple queue pairs and virtual lanes, wherein a given packet payload is stored contiguously in the memory.

Accordingly, Applicant has amended claims 1, 13, 16, 29, 34, and 38 to clarify that InfiniBand payloads are stored contiguously in the memory shared by multiple queue pairs and virtual lanes, wherein a given packet payload is stored contiguously in the memory.

Hence, Applicant respectfully submits that independent claims 1, 13, 16, 29, 34 and 38 as previously presented are in condition for allowance. Applicant also submits that claims 2-12, which depend upon claim 1, claims 14-15, which depend upon claim 13, claims 17-28, which depends upon claim 16, claims 30-33, which depend upon claim 29, claims 35-37, which depend upon claim 34, and claims 39-45, which depend upon claim 38, are for the same reasons in condition for allowance and for reasons of the unique combinations recited in such claims.

CONCLUSION

It is submitted that the present application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

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